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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,109	07/08/2003	Brian James Knight	60707-1420	7691

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EXAMINER	
CHAN, SAI MING	
ART UNIT	**PAPER NUMBER**
2416	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/614,109	KNIGHT ET AL.	
	Examiner	Art Unit	
	Sai-Ming Chan	2416	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Gaytan et al. (U.S. Patent #5638367),** in view of **Priem et al. (U.S. Patent #6023738)**.

Consider **claims 1, 3 and 7,** Gaytan et al. clearly disclose and show a method for transferring network packet data stored in memory to an output device, the method comprising the steps of:

concatenating one or more packet data octets from at least a first data word having at least one packet data octet to be included in a network packet to generate a first sequence of packet data octets having an octet length at least as great as an octet length of a data word (fig. 3 (600), col. 5, lines 51-63 (word packing));

storing the first sequence of packet data octets when the octet length of the sequence of packet data octets is equal to the octet length of a data word (fig. 3 (600), col. 5, lines 51-63 (word packing then transfer to FIFO)); and

an octet length of the first subset of packet data octets is equal to the octet length of a data word (col. 10., lines 52-55 (byte pack data from one word to another)).

However, Gaytan et al. do not specifically disclose storing excess data in alignment register.

In the same field of endeavor, Priem et al. clearly disclose:

storing the first sequence of packet data octets in a FIFO buffer ((fig. 1 (FIFO), column 2, lines 1-9)) operably connected to the output device (fig. 1 (I/O drvice)); and

storing a first subset of packet data octets from the first sequence of packet data octets in the FIFO buffer (col. 2, lines 1-9) and storing a remaining second subset of packet data octets from the first sequence in an alignment register (fig. 1 (overflow), col.

3, col. 4, lines 5-6 (space for overflow)) when the octet length of the first sequence of packet data octets exceeds the octet length of a data word (fig. 1 (overflow), col. 3, col. 4, lines 5-6 (space for overflow so data will not be lost)).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to transfer packet data stored in memory to output device, as taught by Gaytan, and show storing excess data in alignment register, as taught by Priem, so that concatenated data packets of equal length can be stored in the FIFO registers.

Consider **claim 2,** and **as applied to claim 1 above,** Gaytan et al. clearly show the step of storing the first sequence of packet data octets in the alignment register (fig. 6a (63), col. 7, lines 21-31 (64-bit data word)) when the octet length of the first sequence of packet data octets is less than the octet length of a data word (fig. 6a (63), col. 7, lines 21-31 (64-bit data word)).

Consider **claims 5, 9, 10 and 11,** Gaytan et al. clearly show a system for transferring network packet data stored in memory to an output device, the system comprising:

a direct memory access (DMA) (col. 5, lines 52-59 (DMA)) interface for accessing a set of data words stored in memory (col. 2, lines 6-11(words of data)), each data word having at least one valid octet to be included in a network packet (col. 2, lines 6-11(only valid data)) and each data word being accessed using a DMA address associated with

the data word (col. 5, lines 52-59 (DMA));

a first in-first out (FIFO) buffer for storing network packet data to be transmitted by the output device (fig. 3 (280)); and

an alignment block having at least one alignment register (col. 5, lines 52-59), wherein the alignment register for storing at least one data octet (col. 2, lines 6-11(only valid data)), and wherein the alignment block is adapted to:

concatenating one or more packet data octets from at least a first data word having at least one packet data octet to be included in a network packet to generate a first sequence of packet data octets having an octet length at least as great as an octet length of a data word (fig. 3 (600), col. 5, lines 51-63 (word packing));

storing the first sequence of packet data octets when the octet length of the sequence of packet data octets is equal to the octet length of a data word (fig. 3 (600), col. 5, lines 51-63 (word packing then transfer to FIFO)); and

an octet length of the first subset of packet data octets is equal to the octet length of a data word (col. 10., lines 52-55 (byte pack data from one word to another)).

However, Gaytan et al. do not specifically disclose storing excess data in alignment register.

In the same field of endeavor, Priem et al. clearly disclose:

storing the first sequence of packet data octets in a FIFO buffer ((fig. 1 (FIFO), column 2, lines 1-9)) operably connected to the output device (fig. 1 (I/O drvice)); and

storing a first subset of packet data octets from the first sequence of packet data octets in the FIFO buffer (col. 2, lines 1-9) and storing a remaining second subset of

packet data octets from the first sequence in an alignment register (fig. 1 (overflow), col. 3, col. 4, lines 5-6 (space for overflow)) when the octet length of the first sequence of packet data octets exceeds the octet length of a data word (fig. 1 (overflow), col. 3, col. 4, lines 5-6 (space for overflow so data will not be lost)).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to transfer packet data stored in memory to output device, as taught by Gaytan, and show storing excess data in alignment register, as taught by Priem, so that concatenated data packets.

Consider **claim 4,** and **as applied to claim 1 above,**

claim 8, and as applied to claim 5 above,

Gaytan et al. clearly show the octet length of a data word is an integer multiple of four (col. 3, lines 16-18).

Consider **claim 6**, and **as applied to claim 5 above**,

claim 12, and **as applied to claim 9 above**,

claim 13, and as applied to claim 9 above,

Gaytan et al. clearly show the method as described.

However, Gaytan et al. do not specifically disclose storing data in alignment register.

In the same field of endeavor, Priem et al. clearly disclose the alignment block is further adapted to store the first sequence of packet data octets in the alignment

register when the octet length of the first sequence of packet data octets is less than the octet length of a data word (fig. 1 (overflow), col. 3, col. 4, lines 5-6 (space for overflow so data will not be lost); Eaminer notes that the excess could be less than a word and the excess data will be combined with the subsequent incoming data to form a word).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to transfer packet data stored in memory to output device, as taught by Gaytan, and show storing data in alignment register, as taught by Priem, so that concatenated data packets.

Consider **claim 14**, Gaytan et al. clearly show a system for transferring network packet data stored in memory to an output device, the method comprising:

means for (fig. 6a (word packing circuit)) concatenating one or more packet data octets from at least a first data word having at least one packet data octet to be included in a network packet to generate a first sequence of packet data octets having an octet length at least as great as an octet length of a data word (fig. 3 (600), col. 5, lines 51-63 (word packing));

means for (fig. 3 (FIFO)) storing the first sequence of packet data octets when the octet length of the sequence of packet data octets is equal to the octet length of a data word (fig. 3 (600), col. 5, lines 51-63 (word packing then transfer to FIFO)); and

an octet length of the first subset of packet data octets is equal to the octet length of a data word (col. 10., lines 52-55 (byte pack data from one word to another)).

However, Gaytan et al. do not specifically disclose storing excess data in alignment register.

In the same field of endeavor, Priem et al. clearly disclose:

storing the first sequence of packet data octets in a FIFO buffer ((fig. 1 (FIFO), column 2, lines 1-9)) operably connected to the output device (fig. 1 (I/O drvice)); and

means for (fig. 1(FIFO)) storing a first subset of packet data octets from the first sequence of packet data octets in the FIFO buffer (col. 2, lines 1-9) and storing a remaining second subset of packet data octets from the first sequence in an alignment register (fig. 1 (overflow), col. 3, col. 4, lines 5-6 (space for overflow)) when the octet length of the first sequence of packet data octets exceeds the octet length of a data word (fig. 1 (overflow), col. 3, col. 4, lines 5-6 (space for overflow so data will not be lost)).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to transfer packet data stored in memory to output device, as taught by Gaytan, and show storing excess data in alignment register, as taught by Priem, so that concatenated data packets of equal length can be stored in the FIFO registers.

Consider **claim 15**, and **as applied to claim 14 above**, it is being rejected for the same reason as set forth in **claim 2**.

Consider **claim 16**, and **as applied to claim 14 above**, it is being rejected for the same reason as set forth in **claim 3**.

Consider **claim 17**, and **as applied to claim 16 above**, it is being rejected for the same reason as set forth in **claim 3**.

Consider **claim 18**, and **as applied to claim 17 above**, it is being rejected for the same reason as set forth in **claim 3**.

Consider **claim 19**, and **as applied to claim 18 above**, it is being rejected for the same reason as set forth in **claim 3**.

Consider **claim 20**, and **as applied to claim 14 above**, it is being rejected for the same reason as set forth in **claim 4**.

Response to Arguments

Applicant's arguments, with regard to claim 1, under 35 U.S.C. 103(a), filed 3/25/2008 have been fully considered but they are not persuasive.

In the present application, Applicant basically argues, on pages 10-18 of the remarks, that Priem et al., do not teach or suggest "generate a first sequence of packet data", "storing the packet data when it word length" and "a alignment register".

The Examiner has modified the response with a new reference (by the same author, Priem) to provide "generate a first sequence of packet data", "storing the packet data when it word length" and "a alignment register". See the above rejections of claim 1, for the relevant interpretation and citations found in Priem et al., disclosing the limitations.

Conclusion

Any response to this Office Action should be **faxed to** (571) 273-8300 **or mailed to**:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Hand-delivered responses should be brought to

Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sai-Ming Chan whose telephone number is 571-270-1769. The examiner can normally be reached on Monday - Friday 8:00-5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on 571-272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Sai-Ming Chan/
Examiner, Art Unit 2616

January 8, 2009

/Brenda Pham/
Primary Examiner, Art Unit 2416